



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71660 is the latest member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA.

A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system.

Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 71660 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2 as a native interface as well as support for user installed protocols.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Xilinx Virtex-6 FPGA

The Model 71660 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow

FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, QDRII+ SRAM or DDR3 SDRAM memory, PCIe interface, programmable LVDS I/O, gigabit serial interfaces, and clock, gate, and synchronization circuits. The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.

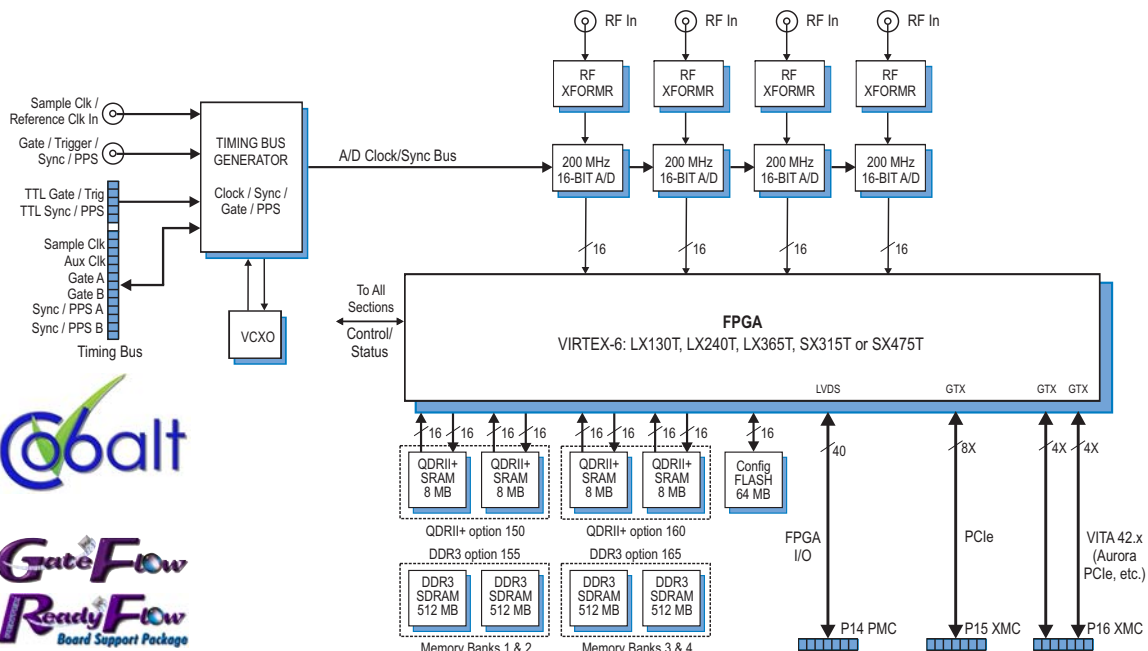
The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 adds the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 adds the P16 XMC connector with dual x4 gigabit links to the FPGA to support serial protocols.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC ➤



XMC Interface

The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual x4 links or a single x8 link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71660 supports x8 PCIe on the first XMC connector leaving the second connector free to support user installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

Model Description

71660 4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC

Options:

-062	XC6VLX240T FPGA
-063	XC6VLX365T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions

connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets.

For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Intelligent DMA Engine

All memory banks are supported with DMA engines for easily moving data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode.

In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing channel ID, a sample-accurate timestamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock Input

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Function: 10 to 800 MHz sample clock or a 5 or 10 MHz system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6

XC6VLX130T

Optional: Xilinx Virtex-6

XC6VLX240T, XC6VLX365T,

XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Installs PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs XMC P16 connector with two 4X serial links to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM Memory Banks

Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks

PCI-Express Interface

PCI Express Bus: Gen. 1 x8 or Gen.2 x4

Environmental

Operating Temp: 0° to 50° C

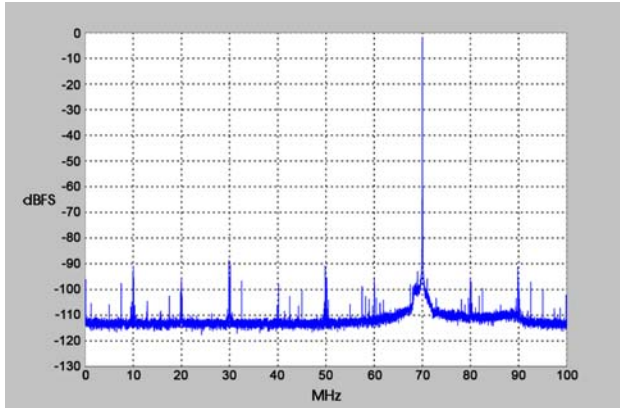
Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

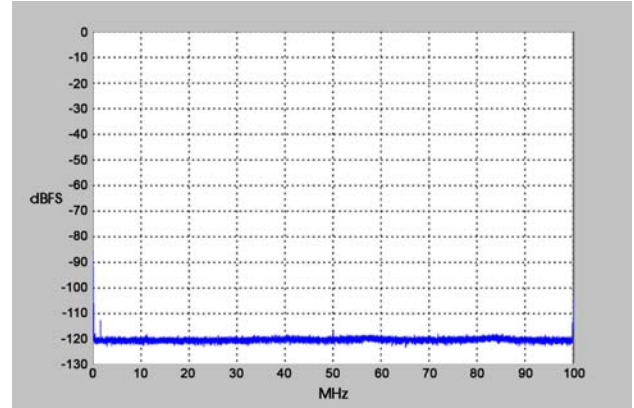
A/D Performance

Spurious Free Dynamic Range



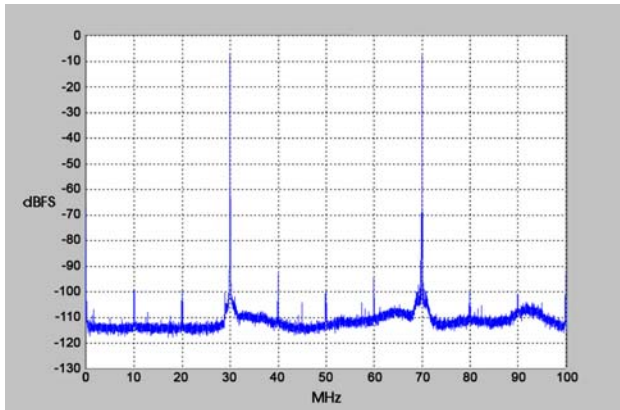
$f_{in} = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$, Internal Clock

Spurious Pick-up



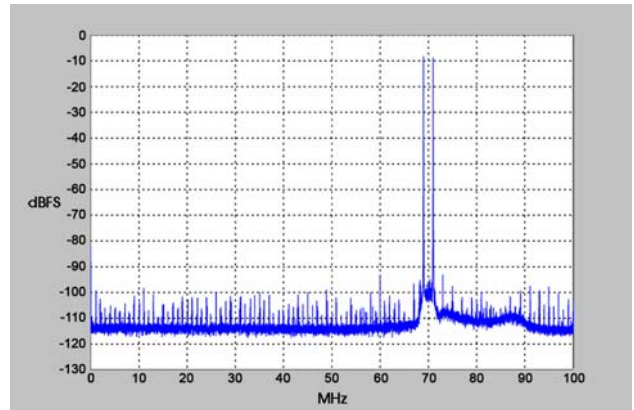
$f_s = 200 \text{ MHz}$, Internal Clock

Two-Tone SFDR



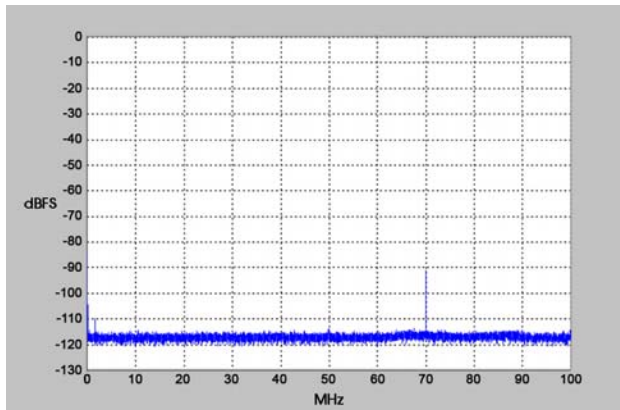
$f_1 = 30 \text{ MHz}$, $f_2 = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$

Two-Tone SFDR



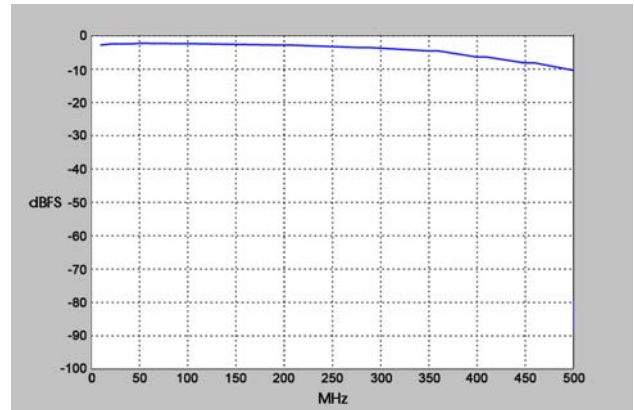
$f_1 = 69 \text{ MHz}$, $f_2 = 71 \text{ MHz}$, $f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$, Ch 1 shown

Input Frequency Response



$f_s = 200 \text{ MHz}$, Internal Clock