

New!



Features

- Complete software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 1 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Clock synthesizer with independent A/D and D/A rates
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71620 is the first member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications and radar system. It includes three A/Ds and two D/A converters and four banks of memory. The Model 71620 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2 as a native interface.

A/D Converter Stage

The front end accepts three full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the

dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

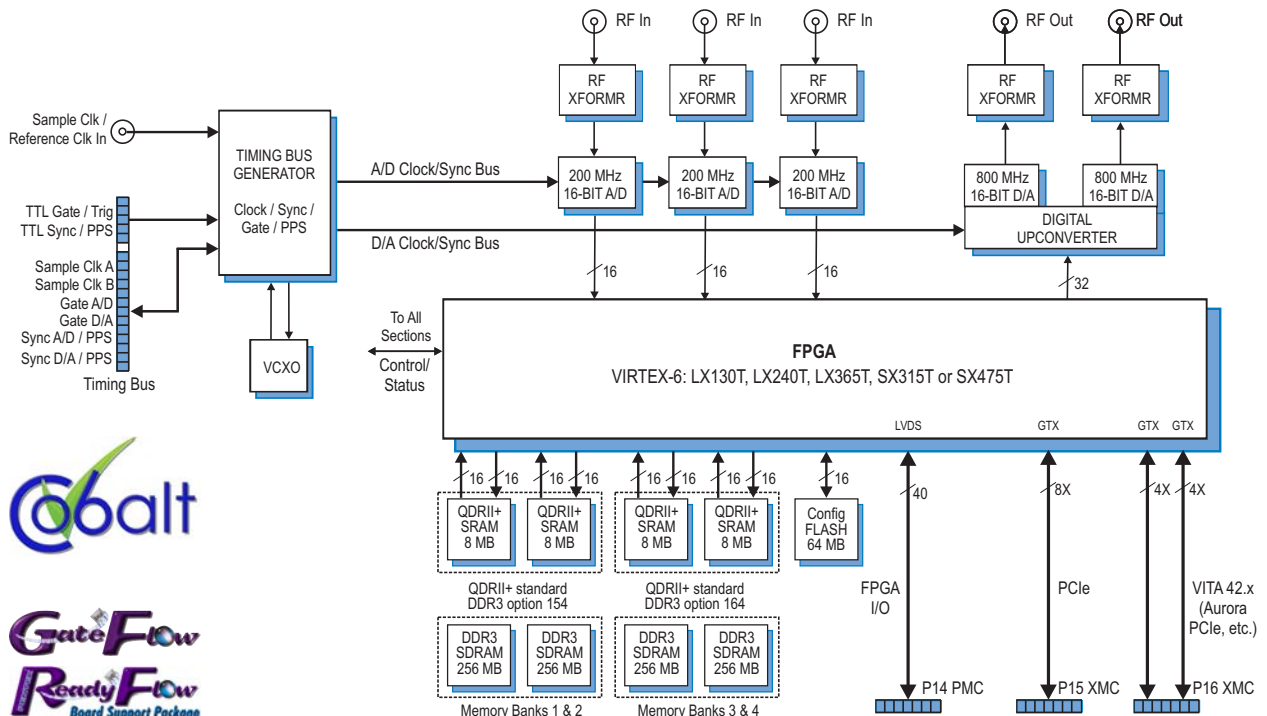
If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Xilinx Virtex-6 FPGA

The Model 71620 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR3 SDRAM or QDRII+ SRAM memory, PCIe interface, programmable LVDS I/O and clock, gate, and synchronization circuits. The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.

The SXT parts feature up to 2016 DSP48E slices and are ideal for ➤



► modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 adds the P14 PMC connector with pairs of LVDS connections to the FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM,

DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 256 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Intelligent DMA Engine

All memory banks are supported with DMA engines for easily moving data through the PCIe interface. For each transfer, the DMA engine can automatically construct metadata packets containing channel ID, a sample-accurate timestamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

XMC Interface

The Model 71620 complies with the VITA 42.0 XMC specification for carrier boards. Two connectors provide dual x4 links or a single x8 link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71620 supports x8 Gen. 2 PCIe on the first XMC connector leaving the second connector free to support user installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71620 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

Model Description

71620 3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - XMC

Options:

-104 FPGA I/O through P14 connector
 -154 DDR3 SDRAM Memory replaces QDRII+ SRAM in Banks 1 and 2
 -164 DDR3 SDRAM Memory replaces QDRII+ SRAM in Banks 3 and 4

Contact Pentek for availability of conduction-cooled versions